ABSTRACT OF THE DISCLOSURE

A method and apparatus for generating clock frequencies using cascaded phase-locked loop (PLL) circuits includes a first PLL circuit coupled to a second PLL circuit to produce a microprocessor I/O data clock signal and a microprocessor core clock signal, respectively. In one embodiment, the first PLL produces the data clock signal based upon a first reference signal and a first feedback signal, where the first feedback signal is derived from the data clock signal. Furthermore, the second PLL circuit produces the core clock signal based at least in part upon a second reference signal and a second feedback signal, where the second reference signal is derived from the data clock signal and the second feedback signal is derived from the core clock signal.